

Amendments to the Specification

The following paragraphs will replace all prior versions in this application.

Replacement Paragraphs

[0009] In a first aspect of the present invention, a method for designing an integrated circuit includes receiving data specifying a plurality of interconnects and components of a design of an integrated circuit and optimizing the design of the integrated circuit. Data specifying the plurality of interconnects and devices of the integrated circuit is optimized based on at least one of interconnect channel capacities bandwidth, scalability, latency, position of devices and interconnect configuration.

[0017] FIG. 2 is an illustration of an embodiment of the present invention wherein a single application specific integrated circuit (ASIC) with configured interconnect channel capacities bandwidth between components is shown;

[0029] There are many varieties of ASIC manufacturing, such as custom built circuits from scratch, which is time consuming and complicated, to using gate arrays, standard cells, programmable logic devices (PLD), customer specific integrated circuits (CSIC), application specified standard products (ASSP), and the like. However, as the number of gates increase, such as gate counts over 50 million, the lack of a comprehensive connectivity that embraces the disparate IP, numerous clock domains, exponential growth of on-chip interconnect channel capacities bandwidth, problems of functional verification as the complexity and number of functional elements grow, and the like, make such a design process exceedingly difficult. Further, current design procedures are implemented without a re-use methodology, thereby limiting current implementations from improving future design implementations.

[0046] Referring now to FIG. 2, an embodiment 200 of the present invention is shown wherein a single application specific integrated circuit (ASIC) with configured interconnect channel capacities bandwidth between components is employed. An ASIC 202 may be configured for a variety of tasks, such as providing functionality to a TV/Set-top box 204, Ethernet 206, and other external device 208 as contemplated by a person of ordinary skill in the art. The ASIC may include a variety of components, such as a microprocessor 210, RAM 212, and the like, which communicate at different target interconnect channel capacities bandwidths.

[0047] By utilizing the present invention, a “wrapper-on-chip bus” (OCB) may be provided around the components to take advantage of and optimally configure interconnect channel capacities bandwidth within the ASIC. For example, interconnect channel capacities bandwidth may be configured when the ASIC components, such as cells, blocks and cores, are built or instantiated within the ASIC, may be configured “on-the-fly” in a FPGA or PLD fashion, and the like as contemplated by a person of ordinary skill in the art. In the illustration shown in FIG. 2, interconnect channel capacities bandwidths are shown with varying degrees of lines with arrows, and control lines, such as for in-band signaling for control instructions both to and from the microprocessor 210 core, are shown with lines without arrowheads.

[0049] Further, the scheme may provide scalability, such as a speed per link, number of links, and the like. For example, to address clock considerations, such as a lower clock speed, 20 links may be provided to achieve the desired interconnect channel capacities bandwidth, for power considerations, a higher clock speed and fewer connections may be utilized.

[0052] Then, interconnect performance and other functionality may be described, as shown in the embodiment depicted in FIG. 5. In this example, an interconnect channel capacities bandwidth is specified for the interconnections indicated in

FIG. 4. For instance, a interconnect channel capacity bandwidth of 2 MB/s may be defined for an interconnect 314 between a processor 316 and RAM 304 by a user, such as by selecting the interconnect 314 and accessing a menu, an input box, and the like. Likewise, the user may continue to specify interconnect performance between other components, such as RAM 304 and the stream manager 306, and the like. It may also be desirable to provide a default for performance between unspecified interconnects, such as an interconnect 318 provided between the stream manager 306 and a hardware protocol engine 320. In this way, a direct connectivity definition for functional components of an ASIC may be achieved. It may also be preferable to enable such undefined interconnects to be configured automatically, as will be discussed later.

[0054] Further, the position of the components, as well as the interconnections between components, may be configured to provide the desired interconnect channel capacity bandwidth as specified by the direct connectivity definition, as well as provide desired latency. Moreover, logic, such as implemented through an agent, may be employed to arrange components so that necessary interconnections are provided, interconnections arranged to minimize interference, and the like as contemplated by a person of ordinary skill in the art.

[0059] For example, referring now to FIG. 10, an exemplary method 1000 of the present invention is shown wherein a design process is suitable for providing an ASIC and for programming a self-programmable device. Components are “dragged-and-dropped” onto a canvas from a template including representations of the desired components 1002, as shown in FIG. 3. Non-core functionality is then defined 1004, such as latency, desired positioning of selected components, and the like. Next, interconnects are specified 1006, which may include desired interconnect channel capacities bandwidth between components, as shown in FIG. 4.

[0060] The non-core functionality, specified interconnects, interconnect channel capacities bandwidth, and the like are then extracted 1008 to a hardware description language format, which may be formatted in C/C++, Verilog, VHDL, and the like. The language may then be utilized both to simulate and synthesize an ASIC 1010, program a self-programmable device 1012, and the like, as contemplated by a person of ordinary skill in the art, without departing from the spirit and scope of the present invention.

[0072] Optimization of the chip may also be based on heuristic knowledge. For example, through monitoring and experience in the utilization of chips, knowledge may be derived pertaining to how the components interact. Thus, the design may be optimized for this interaction. For example, if two functional components were provided, and during operation, the interconnect channel capacities bandwidth required between the components was a target amount, that amount may be provided in subsequent designs involving those components. Likewise, communication between additional components may be examined and utilized in the provision of layout, design and interconnect channel capacities bandwidth provided on a chip.

[0074] Additionally, an agent may be utilized to configure the chip based on heuristics. Through the use of the abstraction language in which interconnections and non-functional component behavior is described between components, the chip itself may achieve optimization through the monitoring of on-chip behavior, such as data transfer and the like. For instance, previously determined routes and interconnections may be optimized by monitoring the past behavior, and then allocating system resources and routing based on that behavior, such as an interconnection between components may be monitored in which the interconnection does not utilize the total available connection based on the route, but another interconnection does not have sufficient resources. Therefore, the interconnections and resource may be optimized so that optimum

performance is achieved by providing the necessary interconnect channel
capacities bandwidth between components.